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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,271	07/03/2003	Uming Ko	TI-35107	4374

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EXAMINER

TRA, ANH QUAN

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/613,271

**Applicant(s)**

KO ET AL.

**Examiner**

Quan Tra

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 July 2003.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-49 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☒ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-49 is/are rejected.  
7) ☒ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 7/3/03 & 10/2/03.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Double Patenting*

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-49 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-57 of copending Application No. 10/616207. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-49 in the present application recite the same scope with claims 1-57.

3. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

### *Claim Objections*

Claim 39, the limitation "said further buffer" should be --said further driver--.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 11-13 and 27-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 is misdescriptive, thereby renders the claim indefinite. It is misdescriptive to recite "each of said register including plurality of data latch structures". The drawings show each latch is a register, not plurality of registers.

Claims 12-13 are rejected as including the indefinites of claim 11.

A similar reason for claims 27-28

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 7, 12, 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (USP 6437623).

As to claims 1, 11 and 14, Hsu et al. discloses in figure 2 a data latch apparatus, comprising: a first latch (21) for latching a data signal; a second latch (24) coupled to the first latch for retaining the data signal while the first latch is inoperative (in sleep mode); a restore device (25) connected between the first and second latches and driven by a first power supply for transferring the data signal from the second latch to the first latch; and the second latch powered

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by a second power supply other than the first power supply (column 6, lines 29-43). As further called in to 11, it is inherent that the circuit comprises plurality of registers (see the title), and it is inherent that the circuit comprises a data process logic (circuit, not shown, that generating the data signal) for performing data processing operations. As further called in for claim 14, column 1, lines 10-20 teaches that circuit figure 2 is used in a wireless device, such as cellular telephone. It is inherent that cellular telephone having an antenna structure for permitting communication via an air interface; a digital data processor (circuit, not shown that having the data retention registers figure 2) for performing digital data processing operations; a wireless communication interface coupled between the antenna structure and the digital data processor for interfacing between the antenna structure and the digital data processor

As to claim 7, figure 2 shows that the second latch is for retaining the data signal while the first latch is inoperative due to removal of power therefrom.

As to claim 12, it is seen as an intended use for using the circuit figure 2 in a microprocessor, a microcontroller, or a digital signal processor.

As to claim 13, figure 2 shows a logic signal path (B1) connected to the restore devices for distributing the first power supply thereto.

As to claim 15, column 1, lines 10-20, teaches that the circuit is used in one of a mobile telephone, a laptop computer and a personal digital assistant.

8. Claims 1 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Zyuban et al. (US 20030188241).

As to claim 1, Zyuban et al. discloses in figure 6b a data latch apparatus, comprising: a first latch (the most left latch) for latching a data signal (I); a second latch (the latch in 60)

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coupled to the first latch for retaining the data signal while the first latch is inoperative (in sleep mode); a restore device (N1-N8) connected between the first and second latches and driven by a first power supply for transferring the data signal from the second latch to the first latch; and the second latch powered by a second power supply other than the first power supply.

As to claim 6, figure 6B shows that second latch includes a node (SCAN\_OUT) for providing the data signal to the restore device, the restore device including a transistor (N7) having a gate connected to the node.

As to claim 7, figure 6B shows that the second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom.

As to claim 8, figure 6B shows that the second latch includes first and second nodes (SCAN\_OUT; SCAN\_OUT\_b) for providing the data signal to the restore device, the restore device including first and second transistors (N7, N3) having respective gates connected to the first and second nodes, respectively.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6437623) in view of Schober (USP 6333656).

As to claim 2, Hsu et al.'s figure 4 further shows the second latch includes a first node (OUT<sub>T</sub>) for providing the data signal to the restore device. Thus, figures 2 and 4 shows all limitations of

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the claim except for “restore device including first and second transistors having respective gates connected to the first node”. However, Shober’s figure 4 shows a Flip Flop circuit having output buffer (M41-M44) coupled to an output of a latch (slave latch) for the purpose of improving the output strength. Therefore, it would have been obvious to one having ordinary skill in the art to add output buffers for the output of Schober’ latch for the purpose of improving the output signal strength. Thus, the modified Hsu et al.’s figure 4 further shows that first and second transistors (transistors in the buffer) having respective gates connected to the first output.

***Allowable Subject Matter***

11. Claims 3-5 and 9-10 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten or amended to overcome the Double Patenting rejection above.

Claims 16-26, 29-38 and 40-49 would be allowable if rewritten or amended to overcome the Double Patenting rejection above.

12. Claims 27-28 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and rewritten or amended to overcome the Double Patenting rejection above.

Claim 39 would be allowable if rewritten or amended to overcome the objection above.

Claims 3-9 and 9-10 would be allowable because the prior art fails to teach or suggest the first latch includes a plurality of transistors, each transistor of the plurality having a gate oxide, the first and second transistors having gate oxides that are thicker than the gate oxides of the plurality of transistors.

Claims 16-26 and 29-30 are and claims 27-28 would be allowable because the prior art fails to teach or suggest first latch including a first plurality of transistors, each transistor of the first plurality having a gate oxide; the second latch including a second plurality of transistors, each transistor of the second plurality having a gate oxide that is thicker than the gate oxides of the first plurality of transistors; the transfer device including a transistor having a gate oxide that is thicker than the gate oxides of the first plurality of transistors.

Claims 31-38 and 40-49 are and claim 39 would be allowable because the prior art fails to teach or suggest a driver coupled to said latch for, while the first logic device is inoperative, driving the data signal as retained in the latch to an input of a second logic device that remains operative while the first logic device is inoperative.

### ***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Quan Tra', with a long horizontal flourish extending to the right.

Quan Tra  
Patent Examiner

September 9, 2004